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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,724	02/28/2002	Moataz A. Mohamed	00CON105P	1708

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EXAMINER
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TSAI, HENRY

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/085,724	Applicant(s) MOHAMED ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11/11/04.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s)    is/are withdrawn from consideration.
- 5) ☐ Claim(s)    is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s)    is/are objected to.
- 8) ☐ Claim(s)    are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on    is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No.   .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. <u>  </u> |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                       | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)                 |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>  </u> | 6) <input type="checkbox"/> Other: <u>  </u>  |

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**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Gageldonk et al. (U.S. Patent Application Publication No. 2002/0042909) (hereafter referred to as Van Gageldonk et al.'909).

Referring to claim 1, Van Gageldonk et al.'909, as claimed, a VLIW processor comprising: first and second register file banks (inside RF1, see Fig. 1), said first register file bank comprising a first plurality of read ports (a portion the output

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ports from RF1, see Fig. 1), and said second register file bank comprising a second plurality of read ports (another portion the output ports from RF1, see Fig. 1); first and second data path blocks (left and right data path blocks UC1 and UC2 connected to RF1, see Fig. 1), said first data path block comprising a first plurality of execution units (ALU1, L/S1, BU1, and MUL1 see Fig. 1), and said second data path block comprising a second plurality of execution units (ALU2, SHU2, and BU2 see Fig. 1); a first plurality of buses (the buses for the inputs and outputs from RF1, see Fig. 1) coupling said first plurality of read ports (a portion of the output ports from RF1, see Fig. 1) to each of said first and second data path blocks (left and right data path blocks UC1 and UC2 connected to RF1, see Fig. 1); a second plurality of buses coupling said second plurality of read ports (another portion the output ports from RF1, see Fig. 1) to each of said first and second data path blocks (left and right data path blocks UC1 and UC2 connected to RF1, see Fig. 1); wherein an operand residing in said first plurality of read ports is concurrently accessed (since UC1 and UC2 share the first register file RF1 see Fig. 1 and paragraph 25, lines 1-3. Note the data bit in a read port of the Van Gageldonk et al.'909's system certainly is concurrently accessed (or shared) by two execution units) by said first plurality of execution units (ALU1, L/S1,

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BU1, and MUL1 see Fig. 1) in said first data path block and by said second plurality of execution units (ALU2, SHU2, and BU2 see Fig. 1) in said second data path block, wherein said VLIW processor does not include a move bus (since as set forth, first and second register file banks are inside RF1, see Fig. 1. A move bus is not required in the Van Gageldonk et al.'909's system).

Referring to claim 7, Van Gageldonk et al.'909, as claimed, a VLIW processor comprising: a plurality of register file banks (inside RF1, see Fig. 1), each of said plurality of register file banks comprising a respective plurality of read ports (the output ports from RF1, see Fig. 1); a plurality of data path blocks (UC1 and UC2, see Fig. 1), each of said plurality of data path blocks comprising a respective plurality of execution units (UC1 comprising: ALU1, L/S1, BU1, and MUL1; and UC2 comprising: ALU2, SHU2, and BU2 see Fig. 1); a plurality of buses (the buses for the inputs and outputs from RF1, see Fig. 1) coupling said plurality of register file banks to each of said plurality of data path blocks; wherein an operand residing in each of said respective plurality of read ports is concurrently accessed (since UC1 and UC2 share the first register file RF1 see Fig. 1 and paragraph 25, lines 1-3. Note the data bit in a read port of the Van Gageldonk et al.'909's system certainly is concurrently

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accessed (or shared) by two execution units) by each of said respective plurality of execution units, wherein said VLIW processor does not include a move bus (since as set forth, first and second register file banks are inside RF1, see Fig. 1. A move bus is not required in the Van Gageldonk et al.'909's system).

Referring to claim 11, Van Gageldonk et al.'909, as claimed, a VLIW processor comprising: first and second register file banks (inside RF1, see Fig. 1), said first register file bank comprising a first plurality of read ports (a portion the output ports from RF1, see Fig. 1), and said second register file bank comprising a second plurality of read ports (another portion the output ports from RF1, see Fig. 1); first and second data path blocks (left and right data path blocks UC1 and UC2 connected to RF1, see Fig. 1), said first data path block comprising a first plurality of execution units (UC1 comprising: ALU1, L/S1, BU1, see Fig. 1), and said second data path block comprising a second plurality of execution units (UC2 comprising: ALU2, SHU2, and BU2, see Fig. 1); a first plurality of buses (the buses for the outputs from RF1, see Fig. 1) coupling said first plurality of read ports to each of said first and second data path blocks; a second plurality of buses (the buses for the outputs from RF1, see Fig. 1) coupling said second plurality of

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read ports to each of said first and second data path blocks; wherein during a single clock cycle (note as a conventional processor, a read is processed during a single clock cycle in the Van Gageldonk et al.'909's system) an operand residing in one of said first plurality of read ports is accessed by only (this is the situation when only UC1 reads RF1 and UC2 does not read RF1) one of said first plurality of execution units (ALU1, L/S1, BU1, see Fig. 1) in said first data path block (UC1 See Fig. 1), wherein said VLIW processor does not include a move bus (since as set forth, first and second register file banks are inside RF1, see Fig. 1. A move bus is not required in the Van Gageldonk et al.'909's system).

Referring to claim 19, Van Gageldonk et al.'909, as claimed, a VLIW processor comprising: a plurality of register file banks (inside RF1, see Fig. 1), each of said plurality of register file banks comprising a respective plurality of read ports (the output ports from RF1, see Fig. 1); a plurality of data path blocks (left and right data path blocks UC1 and UC2 connected to RF1, see Fig. 1), each of said plurality of data path blocks comprising a respective plurality of execution units (UC1 comprising: ALU1, L/S1, BU1, UC2 comprising: ALU2, SHU2, and BU2, see Fig. 1); a plurality of buses coupling said plurality of register file banks to each of said plurality of data path blocks

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(the buses for the inputs and outputs from RF1, see Fig. 1); wherein during a single clock cycle (note as a conventional processor, a read is processed during a single clock cycle in the Van Gageldonk et al.'909's system) an operand residing in one of said respective plurality of read ports is accessed by only one (this is the situation when only UC1 reads RF1 and UC2 does not read RF1 or when only UC2 reads RF1 and UC1 does not read RF1) of said respective plurality of execution units, wherein said VLIW processor does not include a move bus (since as set forth, first and second register file banks are inside RF1, see Fig. 1. A move bus is not required in the Van Gageldonk et al.'909's system).

As to claim 2, Van Gageldonk et al.'909 also discloses: an operand residing in said second plurality of read ports is concurrently accessed (since UC1 and UC2 share the first register file RF1 see Fig. 1 and paragraph 25, lines 1-3. Note the data bit in a read port of the Van Gageldonk et al.'909's system certainly is concurrently accessed (or shared) by two execution units) by said first plurality of execution units (ALU1, L/S1, BU1, and MUL1 see Fig. 1) in said first data path block and by said second plurality of execution units (ALU2, SHU2, and BU2 see Fig. 1) in said second data path block.

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As to claims 3, 8, 15, and 20, Van Gageldonk et al.'909 also discloses: each of said first and second plurality of execution units (ALU1, and MUL1 in UC1; and ALU2 in UC2, see Fig. 1) is selected from the group consisting of an ALU and a multiplier.

As to claims 4, 9, 16, and 21, Van Gageldonk et al.'909 also discloses: said first register file bank (a portion of RF1, see Fig. 1) comprises a first plurality of write ports (see Fig. 1 and paragraph 25, lines 25-29), and wherein said second register file bank (another portion of RF1, see Fig. 1) comprises a second plurality of write ports (see Fig. 1 and paragraph 25, lines 25-29).

As to claims 5, 10, and 17, Van Gageldonk et al.'909 also discloses: a result of an operation performed in said first data path block (UC1, see Fig. 1) is accessed only (this is the situation when only UC1 writes back to RF1 and UC2 is not in write back stage) by said first plurality of write ports without being accessed by said second plurality of write ports.

As to claims 6, and 18, Van Gageldonk et al.'909 also discloses: a result of an operation performed in said second data path block (UC2, see Fig. 1) is accessed only (this is the situation when only UC2 writes back to RF1 and UC1 is not in write back stage) by said second plurality of write ports without being accessed by said first plurality of write ports.

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As to claim 12, Van Gageldonk et al.'909 also discloses:  
during said single clock cycle an operand residing in one of said first plurality of read ports is accessed by only (this is the situation when only UC2 reads RF1 and UC1 does not read RF1) one of said second plurality of execution units in said second data path block.

As to claim 13, Van Gageldonk et al.'909 also discloses:  
during said single clock cycle an operand residing in one of said second plurality of read ports is accessed by only one (this is the situation when only UC1 reads RF1 and UC2 does not read RF1) of said first plurality of execution units in said first data path block.

As to claim 14, Van Gageldonk et al.'909 also discloses:  
during said single clock cycle an operand residing in one of said second plurality of read ports is accessed by only (this is the situation when only UC2 reads RF1 and UC1 does not read RF1) one of said second plurality of execution units in said second data path block.

As to claim 22, Van Gageldonk et al.'909 also discloses:  
during said single clock cycle an operand residing in one of said respective plurality of read ports is accessed by only one (this is the situation when only UC1 reads RF1 and UC2 does not read

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RF1 or when only UC2 reads RF1 and UC1 does not read RF1) of said respective plurality of execution units.

***Response to Amendment***

3. Applicant's arguments filed 11/11/04 have been fully considered but they are not deemed to be persuasive.

Applicants argue that Van Gageldonk does not disclose, teach, or suggest the VLIW processor of the present embodiment. Van Gageldonk does not disclose, teach, or suggest a VLTW processor that does not include or utilize "move buses," as claimed in amended independent claims 1, 7, 11, and 19 (page 16/18, last three lines). Examiner disagrees with Applicants. As set forth in the art rejections above, Van Gageldonk et al.'909, as claimed, a VLIW processor (see Fig. 1) comprising: first and second register file banks (inside RF1, see Fig. 1) wherein said VLIW processor does not include a move bus (since as set forth, first and second register file banks are inside RF1, see Fig. 1. A move bus is not required in the Van Gageldonk et al.'909's system).

Van Gageldonk et al.'909 anticipates the claimed invention.

**Conclusion**

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


**Contact Information**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful,

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the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100.

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 703-872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI  
PRIMARY EXAMINER

December 27, 2004